Noise Model for Multiple Segmented Coupled *RC* Interconnects

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Abstract

Performance of high-speed VLSI circuits is increasingly limited by interconnect coupling noise. We present simple and improved analytical models for noise phenomena due to coupling capacitance. We extend the Π model presented in [4] to accommodate a *segmented aggressor*. We also include a linear driver resistance in the modeling of both victims and aggressors to measure their estimate on peak noise. Finally, we extend this model to *multiple segmented aggressors* by superposing noise contributions of individual aggressors and sweeping the result in the time domain to determine peak noise (in contrast to adding the individual peak noise values for individual aggressors). Accuracy in the results depends greatly on actual positioning of victim-aggressor overlaps. We find that previous models that assume aggressors run parallel to the victim net for its entire length do not yield peak noise results nearly as close to SPICE-computed values. We also find that inclusion of driver resistance in the model improves accuracy. Our noise model for a single segmented aggressor is within $\sim$ 16% of SPICE. Results for two segmented aggressors are within acceptable tolerances with respect to SPICE, but error increases with the number of aggressors. We note that these results are almost always pessimistic.

1 Introduction

The increasing significance of crosstalk between parallel *RC* interconnect lines in high-speed, high-density VLSI designs is well recognized [1] [7]. Crosstalk effects due to capacitive coupling between lines increase with the average length of interconnects (relative to minimum feature size), the density of interconnect routings (due to higher aspect ratios enabled by improved lithographic processes), and the switching speed of devices. High-speed circuits (such as dynamic circuits and latches) exhibit noise sensitivity at both input and output nodes, which makes accurate noise coupling analysis critical for design.

"Filtering" methodologies for signal integrity verification attempt to confirm noise peaks on sensitive nodes to be below recommended threshold levels as early in the design process as possible. After detailed routing, it is possible to extract a detailed coupled *RC* network for all signal lines and perform detailed dynamic (e.g., SPICE) simulations. However, in general for advanced processor designs with shorter (and more) critical paths, SPICE simulations are prohibitively expensive. Before detailed routing, there are issues of information quality and completeness in the parasitic database, since only probabilistic or approximate embedding of wires are available. We observe that there are two limiting factors in the noise analysis: (1) the amount of data available, and (2) the models that can do noise estimate on that data. In this work, we focus on the modeling issue.

Today's early noise analysis tools employ a technique which takes the coupling capacitance to be some multiple of ground capacitance depending upon the switching conditions. A single effective capacitance value for the interconnect is computed for use in delay estimation. This is multiplied by a *switching factor*, which is often taken to be slightly more than zero for a pair of lines switching in the same direction, and slightly less than two for a pair of lines switching in the opposite direction. The downside of this simple technique is that it can lead to highly optimistic or pessimistic estimates of noise and delay. On the other hand, as noted above, full-chip extraction followed by SPICE-based identification of noise- and delay-sensitive nodes is not feasible. Thus, we require a noise model that can estimate noise given the configuration of the interconnects and a quick estimate of parasitics in the circuit. This motivates the development of more accurate predictors of coupling-induced noise and delay based on coupling capacitance values and switching activity (slew times, offsets).

A number of previous works model the effects of interconnect fringing and coupling capacitance on crosstalk. [8] proposes detailed noise analysis using full-chip parasitic extraction and models order reduction to compress parasitic data. Coming after physical design, this is computationally expensive and identifies noise problems too late in the design cycle. The approach of [3] uses a detailed victim net analysis but applies an infinite ramp instead of a finite ramp as input to the aggressor net. To simplify the analysis further, each coupling capacitor is replaced by a current source whose value is slew rate (i.e., slew rate of aggressor source voltage) times the coupling capacitance. It is implicitly assumed that the aggressor signal slope does not degrade downstream from the aggressor source. Hence, for longer lines this approach can produce either overestimated or underestimated peak noise values.

Sakurai [9] solves partial differential equations for coupled *RC* lines to derive noise and delay expressions. However, driver modeling is not considered and the analysis is limited to step response. Kawaguchi and Sakurai [5] use the diffusion equation to analyze

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capacitively coupled interconnects, but also consider only the case of a step input. Different peak noise expressions are derived for various combinations of driver resistance to wire resistance ratio and load capacitance to wire capacitance ratio. [10] uses an L model for RC interconnects and obtains noise bounds for the case of a step input only. However, the model does not take into account the interconnect resistance while deriving noise expressions, and various assumptions (e.g., $R_{driver} \ll R_{int}$ and $C_{load} \ll C_{int}$) are made in deriving expressions for noise and delay. Nakagawa et al. [6] use an L model for interconnects to compute peak noise expressions under ramp inputs. They derive the slew time at the output of aggressor driver as a function of input slew time of the driver, intrinsic gate delay, and gate load delay considering effective capacitance seen by the driver. However, they assume that peak noise always occurs after time $t \geq T_S$, where T_S is slew time at the output of the aggressor driver. [4] present analytical models for peak noise and delay uncertainty for two parallel aggressors of similar configuration. However, their results assume driver resistance to be zero, and no extension to analysis of segmented multiple aggressors[1] is given. Alignment of multiple aggressors is considered in detail by [2], which finds each aggressor's individual peak noise contribution and then aligns aggressors according to timing windows to determine peak noise. However, their work does not focus on how to model an individual segmented aggressor's peak noise.

Contributions of This Work

In this paper, we present simple and improved analytical models for noise phenomena due to coupling capacitance. The improved accuracy of our estimators can (i) be useful in analyzing the sensitivity of circuit performance to various interconnect tuning parameters, and (ii) lead to less over-design and guard-banding at all stages of a performance-convergent synthesis and layout methodology for high-performance designs.

Our specific contributions are as follows. First, we extend the Π model presented in [4] to accommodate a segmented aggressor. Second, we include a linear driver resistance in the modeling of both victim and aggressor to capture its impact on peak noise. Finally, we extend our model to multiple segmented aggressors by adding the noise of individual aggressors and sweeping their noise results in the time domain to determine peak noise (in contrast to adding the individual peak noise values for individual aggressors). Our results indicate that previous models that assume that aggressor interconnects run parallel to the victim net for its entire length do not yield peak noise results close to SPICE, and must be extensively tuned to accommodate various overlaps of victim and aggressors. We also find that inclusion of driver resistance in the model improves results substantially. Last, we observe that instead of adding the peak noise contributions of the individual aggressors, sweeping a superposition of analytical time domain voltage functions that include noise response yields a closer estimate of actual peak noise.

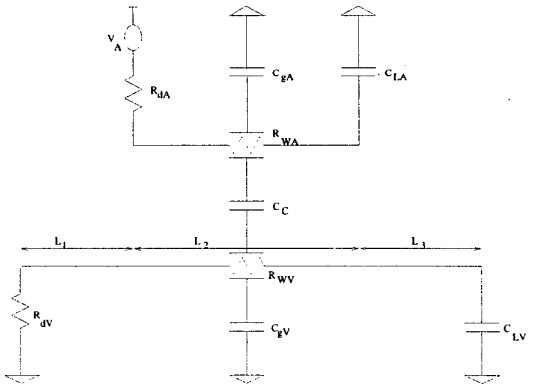

Figure 1: Two parallel segmented coupled interconnects, with victim driver modeled as a linear resistance and aggressor driver modeled as a voltage source and a linear resistance. The load for both victim and aggressor is modeled as a capacitance to ground. This configuration is used for our analysis of peak noise on the victim. Nomenclature: L_1: fraction of victim to the left of aggressor overlap; L_2: fraction of victim overlapped by aggressor; L_3: fraction of victim to the right of aggressor overlap ($L_1 + L_2 + L_3 = 1$); $R_{dA}(R_{dV})$: aggressor (victim) driver resistance; $C_{gA}(C_{gV})$: aggressor (victim) capacitance to ground; $C_{LA}(C_{LV})$: aggressor (victim) load capacitance; C_c: coupling capacitance.

2 Our Model for Segmented Coupled Interconnects

We consider two parallel coupled interconnects with victim driver modeled as a driver resistance only, and aggressor driver modeled as voltage source and driver resistance, as shown in Figure 1. (This is for the case when the victim line is quiet and aggressor line changes from 0 to VCC, inducing noise voltage on the victim line via capacitive coupling. As a result of victim line resistance and the driver resistance, the induced voltage undergoes exponential decay. If the induced voltage is higher and lasts longer (i.e., its pulse width is greater) than certain minimum values, then the destination gate generates a glitch and causes a logical error). For both the victim and the aggressor, the destination gate is modeled as a load capacitance to ground. To simplify analysis, we use an equivalent Π model circuit for the interconnects as shown in Figure 2. We analyze noise at the end of the interconnects. The transformation from Figure 1 to 2 is discussed in detail below.

Our goal is to develop models to estimate peak noise on the victim line for different configurations of the aggressor victim overlaps. We vary the lengths L_1, L_2 and L_3 to generate various overlap configurations. As explained in Figure 1, L_1 refers to the fraction of the victim wire to the left of the overlap between the victim and the aggressor; L_2 refers to the section of the victim wire that overlaps with the aggressor (note that this length corresponds to the length of the aggressor wire); and L_3 refers to the section of the victim wire to the right of the aggressor wire and victim wire overlap. We consider only cases where the victim wire is longer than the aggressor

[1] An aggressor is called a *segmented aggressor* if it overlaps with the victim interconnect for only part of the victim's length, at some given displacement from the victim.

wire.

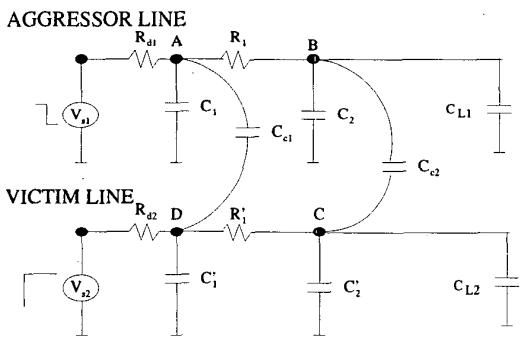

Figure 2: Equivalent circuit (using Π model for interconnect) for the configuration of Figure 1.

After applying the Π model for interconnect as shown in Figure 2, we calculate the peak noise voltage on the victim via the solution given in [4], i.e., the peak noise at the receiver end of the victim net is given by

$$v_C(t_{peak}) = \frac{v_0}{b_2}\left(k_1 e^{s_1 t_{peak}} + k_2 e^{s_2 t_{peak}}\right) \quad (1)$$

(Refer to [4] for a detailed derivation.) Thus, the key to solving for noise in the Figure 1 configuration is to reduce it to the model of [4] (Figure 2). We cannot use that model directly in our current scenario because (1) the model of [4] considers driver resistance to be zero; (2) the resistances from non-overlap regions of the victim wire would isolate various capacitances and force non-uniform distribution of ground and coupling capacitances of the victim wire in contrast to the model of [4]; and (3) the victim wire resistance would vary significantly (and proportionately) with L_2. The Π model to which we reduce our input configuration must address these considerations appropriately. We discuss the transformations required, and the reductions made to input configuration parasitics in defining our Π model, in the next section.

3 Model Transformations

To analyze the segmented configuration, the closest model would be a 3-Π model as shown in Figure 3. Extending the model used in [4] in this way avoids the drawbacks of the 1-Π model in Figure 2. However, the resulting analytical model, and analytical expressions for noise and delay, become excessively complicated. Our approach, therefore, is to transform the parameters of the segmented configuration into the existing simplistic and fast model of [4] (Figure 2). In this section, we present the transformations that we use to reduce the input circuit (Figure 1) to the 1-Π model (Figure 2); these yielded the closest results to SPICE[2] among all the variants that we tried. Our discussion attempts to give the physical intuition behind the various transformations.

[2]We used a distributed multiple-node (more than 45 nodes) SPICE model to compare our results to the 1-Π model. We did not compare our model with a 1-Π SPICE model. Thus, in effect, our model is a reduction of a 45+ node distributed SPICE model to a fast analytical 1-Π model.

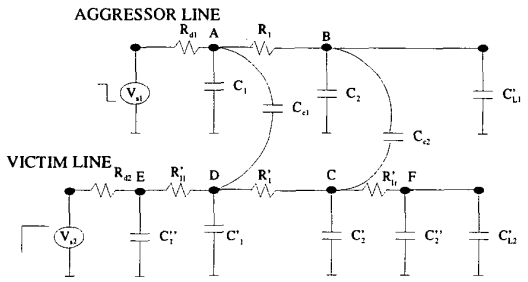

Figure 3: Equivalent circuit (using 3-Π model for interconnect) for the configuration of Figure 1.

- **Victim wire resistance transformations.** The current being charged into the victim wire from the aggressor coupling capacitance discharges from the keeper end of the victim wire. Thus, the victim wire resistance that actually plays a role in discharge of the victim current is the resistance from the keeper (driver) end of the victim to the overlap region between the victim and the aggressor (the last leg of the coupling capacitance pumping charge into the victim wire). In other words, the victim wire resistance in the model should correspond to the lengths due to L_1 and L_2 fraction of the victim wire. However, in order to be close to the extended 3-Π model, we consider the victim wire resistance to correspond to the length of the overlap between the victim and the aggressor (L_2), and model the resistance due to fraction L_1 of the victim wire as part of the driver resistance of the model (see victim driver resistance transformations below). Thus, we transform the victim wire resistance as $R'_1 = R_{wv} * L_2$.

- **Victim driver resistance transformations.** As explained above, we transform the victim driver resistance to also include the resistance of the victim net to the left of the overlap region of victim and the aggressor. I.e., $R_{d2} = R_{dv} + L_1 * R_{wv}$. The reason for this is that the ground node to the left of the victim driver resistance (that keeps the victim peak voltage) is isolated from the left coupling cap leg of the Π model by these resistances, and can thus be modeled as the driver resistance of the victim keeper.

- **Victim ground capacitance transformations.** In our Π model, we distribute the ground capacitance of the victim net non uniformly between the left and the right leg of the Π. The reason is that in light of uneven overlap between victims and aggressors, the ground capacitance on the right end of the Π model is isolated by the resistance on the victim net. However, the whole of the ground capacitance is actually available to discharge the noise pulse from the aggressor. Thus, we distribute the victim net's ground capacitances as:

  $C'_1 = 0.5 * C_{gV} * (1 + L_1 - L_3)$
  $C'_2 = 0.5 * C_{gV} * (1 - L_1 + L_3)$

- **Coupling capacitance transformations.** In the real configuration (Figure 1), the coupling capacitance starts L_1 distance

away from the keeper end of the victim net; in our Π model (Figure 2), the left leg of the coupling capacitance C_{c1} is at the keeper end of the victim net. This discrepancy between model and real circuit pushes the keeper end of the victim net closer to zero potential, causing more discharge from the left leg of the coupling capacitance in the model than in the real circuit (because in the real circuit, the capacitance is isolated by the wire resistance). Therefore, we lower the coupling capacitance on the keeper end of the victim net:

$$C_{c1} = 0.5 * C_c * (1 - L_1)$$
$$C_{c2} = 0.5 * C_c * (1 + L_1)$$

To extend our model to capture multiple aggressors' noise impact on the victim net, we first transform the input parameters of each aggressor to that individual aggressor's Π model with victim net. We then compute the time domain function for each aggressor's noise impact using the noise voltage function derived in [4]. Next, to find the peak noise value due to all aggressors, we sweep the noise value of each aggressor in time domain and add all individual noise contributions. The peak noise value reported is the maximum attained by this superposition of noise contributions.

4 Simulation Results

Cases	width (in μm)	spacing (in μm)	Victim length (in μm)
1	0.49	0.46	1000
2	0.49	0.46	5000
3	1.00	0.46	10000
4	0.49	1.30	1000

Cases	R_{ini}/length (in Ω/mm)	C_{gnd}/length (in fF/mm)	C_{coup}/length (in fF /mm)
1	122.9	63.2	115.02
2	122.9	63.154	115.006
3	60.53	98.397	118.0
4	122.9	109.3	46.2

Table 1: Interconnect parameters used in various SPICE simulations (C_L = 153 fF due to inverter gate capacitance for all cases).

To validate our new analyses, we have considered two adjacent $M3$ interconnects from a real microprocessor design in 0.25 μm CMOS technology. We assume a victim interconnect with properties shown in Table 1, driven by an inverter with resistance R_{dV} = 10Ω. We study various configurations of victim interconnect length, width, and spacing as shown in Table 1. For all such victim interconnects, aggressors with identical width and spacing but varying overlap are considered, in order to study the effect of aggressor segmentation on victim noise. This segmentation [overlap] of aggressors is fully specified by L_1, L_2 and L_3, as explained earlier. To evaluate the effectiveness of the model, simulation results and comparisons against SPICE are tabulated for three representative configurations of aggressor segmentation:
Config. I: L_1 20%, L_2 60%, L_3 20% [Figure 1, Table 2]
Config. II: L_1 0%, L_2 60%, L_3 40% [Figure 4, Table 3]
Config. III: L_1 40%, L_2 60%, L_3 0% [Figure 5, Table 4]

The aggressor driver resistance is assumed to be R_{dA} = 100Ω. We also assume that the loads at the end of the lines are identically sized inverters, modeled as pure capacitances. We note that the model proposed above is extremely efficient to evaluate (despite sometimes long arithmetic expressions), with negligible run times in comparison to SPICE run times.

	$T_S = 1\ ps$			$T_S = 100\ ps$		
Cases	SPICE	Our Model	% Error	SPICE	Our Model	% Error
1	0.255	0.269	5.67	0.180	0.197	9.61
2	0.515	0.462	-10.42	0.506	0.459	-9.36
3	0.520	0.460	-11.52	0.526	0.459	-12.68
4	0.103	0.109	5.65	0.072	0.079	10.66

	$T_S = 200\ ps$			$T_S = 400\ ps$		
Cases	SPICE	Our Model	% Error	SPICE	Our Model	% Error
1	0.114	0.119	4.84	0.058	0.061	4.56
2	0.490	0.451	-8.00	0.436	0.421	-3.51
3	0.521	0.457	-12.22	0.502	0.450	-10.52
4	0.046	0.048	4.98	0.023	0.025	4.57

Table 2: Peak noise results for configuration I L_1: 20% L_2: 60% & L_3: 20%. See Figure 1.

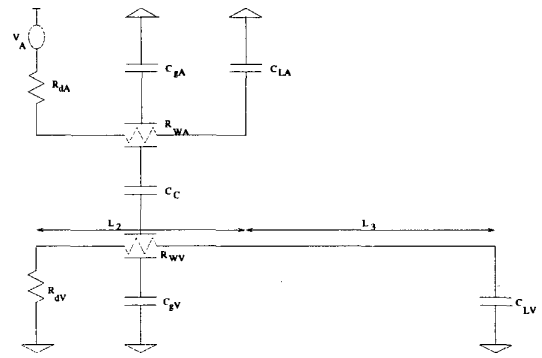

Figure 4: Configuration II L_1: 0% L_2: 60% & L_3: 40%. This configuration corresponds to the aggressor overlapping towards the receiver node of the victim net.

Our simulation results in Tables 2, 3 and 4 indicate that our model transformations yield close results to SPICE simulations. The maximum error reported is ~ 16%.

Simulation Results for Multiple Aggressors

We have performed experiments with up to three aggressors. As explained in Section 3, we report peak noise values resulting from superposition of individual aggressors' noise contributions. Given the degree of freedom in choosing L_1, L_2 and L_3 for each of the aggressors, the number of combinations of the aggressors' locations with respect to victim driver and receiver increases exponentially with the number of aggressors. To test our model, we limited the resolution on L_1, L_2 and L_3 to 20% of the victim wire length. Our experiments enumerate all the possible combinations of aggressor configurations with respect to victim, for two and three aggressors. For this, we vary each aggressor's L_1 and L_3 from 0% to 80%, and L_2 from 20% to 100% in steps of 20% aggressor length. Figure 6 explains one example two-aggressor configuration, and Table 5

Cases	$T_S = 1\ ps$			$T_S = 100\ ps$		
	SPICE	Our Model	% Error	SPICE	Our Model	% Error
1	0.220	0.244	11.29	0.153	0.168	10.10
2	0.385	0.355	-7.89	0.377	0.352	-6.77
3	0.393	0.349	-11.13	0.391	0.349	-10.84
4	0.087	0.097	11.01	0.061	0.067	10.47

Cases	$T_S = 200\ ps$			$T_S = 400\ ps$		
	SPICE	Our Model	% Error	SPICE	Our Model	% Error
1	0.097	0.098	1.02	0.050	0.050	0.001
2	0.364	0.343	-5.94	0.320	0.311	-2.62
3	0.388	0.346	-10.67	0.373	0.338	-9.46
4	0.038	0.039	1.16	0.020	0.020	0.02

Table 3: Peak noise results for configuration II L_1: 0% L_2: 60% & L_3: 40%. See Figure 4.

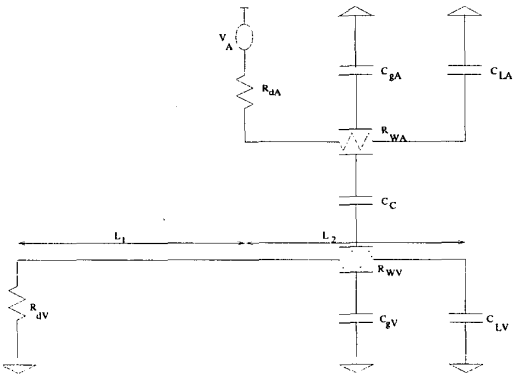

Figure 5: Configuration III L_1: 40% L_2: 60% & L_3: 0%. This configuration corresponds to the aggressor overlapping towards the driver node of the victim net.

summarizes the results for this case. Similarly, Table 6 summarizes the results for one example three-aggressor case. Maximum error in peak noise for the example two-aggressor case shown in Figure 6 is $\sim$ 17% (Table 5), and $\sim$ 30% for the example three-aggressor case (Table 6). Overall, we find that for a small number of the aggressor configurations, the error can be higher than that seen for the examples in Tables 5 and 6. In most cases, the error is on the side of pessimism.

5 Conclusions

In conclusion, we have analyzed the accuracy and applicability of new, very simple closed-form models and their transformations for computing crosstalk noise pulse peak and width for deep-submicron interconnects. Specifically, we have provided simple to use reductions and transformations into an existing model, to enable accurate peak noise (and noise pulse width) modeling for more realistic interconnect configurations (i.e., segmented aggressors and multiple aggressors). We find that our model transformations give results within $\sim$ 16% of the SPICE results for various configurations of a single aggressor-victim pair. Applying superposition, our model provides results within reasonable tolerances of SPICE results for two-aggressor and three-aggressor cases. The

Cases	$T_S = 1\ ps$			$T_S = 100\ ps$		
	SPICE	Our Model	% Error	SPICE	Our Model	% Error
1	0.281	0.291	0.75	0.205	0.221	8.27
2	0.594	0.536	-0.99	0.618	0.533	-13.77
3	0.640	0.543	-15.08	0.647	0.543	-16.17
4	0.118	0.119	0.76	0.083	0.09	9.19

Cases	$T_S = 200\ ps$			$T_S = 400\ ps$		
	SPICE	Our Model	% Error	SPICE	Our Model	% Error
1	0.130	0.140	7.06	0.067	0.073	7.86
2	0.602	0.526	-12.62	0.535	0.500	-6.61
3	0.641	0.541	-15.66	0.618	0.534	-13.6
4	0.053	0.058	7.30	0.017	0.018	7.88

Table 4: Peak noise results for configuration III L_1: 40% L_2: 60% & L_3: 0%. See Figure 5.

Cases	$T_S = 1\ ps$			$T_S = 100\ ps$		
	SPICE	Our Model	% Error	SPICE	Our Model	% Error
1	0.469	0.532	13.44	0.336	0.39	16.20
2	0.756	0.816	5.8	0.742	0.811	6.92
3	0.85	0.893	5.03	0.857	0.891	3.98
4	0.196	0.215	9.7	0.14	0.157	12.82

Cases	$T_S = 200\ ps$			$T_S = 400\ ps$		
	SPICE	Our Model	% Error	SPICE	Our Model	% Error
1	0.222	0.237	6.78	0.117	0.122	4.66
2	0.726	0.793	7.17	0.658	0.732	9.85
3	0.851	0.887	4.57	0.828	0.872	5.41
4	0.091	0.096	5.54	0.047	0.049	4.59

Table 5: Peak noise results for example Two-Aggressor Configuration – Aggressor I: L_1: 0% L_2: 60% & L_3: 40% Aggressor II: L_1: 40% L_2: 60% & L_3: 0%. See Figure 6.

reduction of a detailed distributed victim and aggressor *RC* coupled circuit to a reasonably accurate transformed model has lots of advantages in analysis and estimate methodology. Such transformations are useful for both signal integrity analysis, interconnect/gate load delay computation and finally for delay uncertainty computation.

The approaches described in our paper potentially form the basis of a set of analytical tools to estimate noise peaks early in the ASIC physical implementation flow. We hope to extend our models and results to build a system which can read in an extracted layout, convert the various net overlap configurations to individual victim-aggressor pairs using our transformations, and then report estimates of peak noise, pulse width, delay, slew degradation and effective switching factor for various nets of the layout. Our ongoing work addresses the erroneous behavior of our noise model for the few cases which exhibit high error. We also seek to make this model more scalable (i.e., accurate even with many aggressors) and applicable to aggressors that have opposite-direction drive with respect to the victim.

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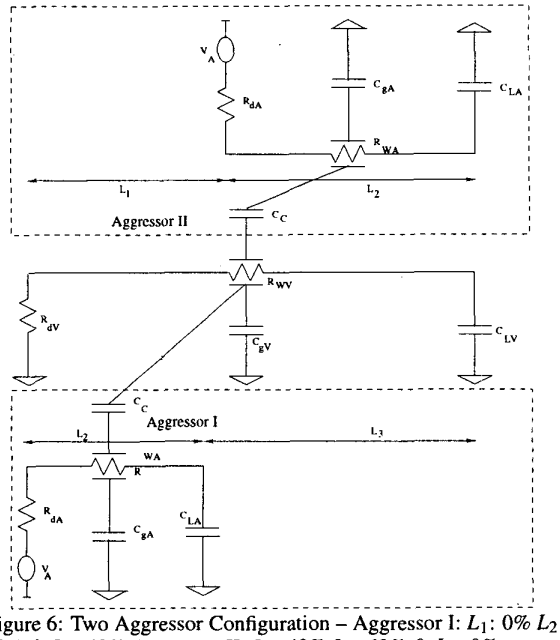

Figure 6: Two Aggressor Configuration – Aggressor I: L_1: 0% L_2: 60% & L_3: 40% Aggressor II: L_1: 40% L_2: 60% & L_3: 0%

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Cases	$T_S = 1\ ps$			$T_S = 100\ ps$		
	SPICE	Our Model	% Error	SPICE	Our Model	% Error
1	0.548	0.698	27.32	0.389	0.473	21.61
2	0.977	1.232	26.05	0.962	1.22	26.76
3	0.981	1.237	26.13	0.992	1.234	24.48
4	0.236	0.276	16.66	0.165	0.189	14.73

Cases	$T_S = 200\ ps$			$T_S = 400\ ps$		
	SPICE	Our Model	% Error	SPICE	Our Model	% Error
1	0.258	0.279	8.12	0.136	0.143	4.64
2	0.963	1.186	26.66	0.85	1.074	26.33
3	0.106	0.112	24.63	0.952	1.193	25.28
4	0.984	1.226	6.02	0.055	0.057	4.61

Table 6: Peak noise results for example Three-Aggressor Configuration – Aggressor I: L_1: 0% L_2: 40% & L_3: 60% Aggressor II: L_1: 20% L_2: 60% & L_3: 20% Aggressor III: L_1: 60% L_2: 40% & L_3: 0%.